Claim Amendments

Claim 1 (original): A timing distribution apparatus comprising:

a source for producing a signal;

a first filter for removing jitter from the signal; and

a second filter for removing wander from the signal separate and apart from the first filter.

Claim 2 (currently amended): An apparatus as described in Claim 1 wherein the first filter includes a first tuneable directed digital synthesizer connected to the source for producing a first clock signal derived from the signal from the source.

Claim 3 (original): An apparatus as described in Claim 2 wherein the source includes an oscillator that produces the signal.

Claim 4 (currently amended): An apparatus as described in Claim 3 wherein the first filter includes a reference input clock signal mechanism for providing a reference input clock signal with respect to the first clock signal.

Claim 5 (currently amended): An apparatus as described in Claim 4 wherein the first filter includes a first comparison mechanism which accumulates error between the first clock signal and a reference input clock signal and produces an error correction signal to tune the directed digital synthesizer.

Claim 6 (currently amended): An apparatus as described in Claim 5 wherein the first comparison mechanism includes a microcontroller which accumulates the error between the first clock signal and the reference input clock signal for a predetermined number of consecutive cycles, and applies dithering to the accumulated error to produce the error correction signal.

Claim 7 (original): An apparatus as described in Claim 6 wherein the second filter includes a second tuneable directed digital synthesizer connected to the first filter for producing a second clock signal from the first clock signal from the first filter.

Claim 8 (original): An apparatus as described in Claim 7 wherein the second filter includes a second comparison mechanism which accumulates error between the first clock signal and the second clock signal and produces a second error correction signal to tune the second directed digital synthesizer.

Claim 9 (original): An apparatus as described in Claim 8 wherein the first filter removes noise greater than 1 KHz from the signal and the second filter removes noise less than 1 KHz from the signal.

Claim 10 (original): An apparatus as described in Claim 9 wherein the second comparison mechanism includes a second microcontroller which accumulates the error between the first clock signal and the second clock signal for a predetermined number of consecutive cycles and computes the second error correction signal.

Claim 11 (previously presented): An apparatus as described in Claim 10 wherein the first comparison mechanism includes a first counter which receives the reference input signal and counts a second predetermined number of cycles between rising edges of the reference input clock signal; a second counter which receives the clock signal and counts the second predetermined number of cycles between rising edges of the clock signal; and a

comparator which compares the counts of the first and second counters and reports differences in the counts every predetermined period to the first microcontroller.

Claim 12 (previously presented): An apparatus as described in Claim 11 wherein the reference input clock signal and the clock signal have a frequency of about 8 KHz, the second predetermined number of cycles is 80 MHz, the predetermined period where the comparator reports differences in the counts to the first microcontroller is about 125 microseconds, and the predetermined number of cycles is 1024.

Claim 13 (original): An apparatus as described in Claim 12 wherein the accumulated error includes a scaled error, and the first microcontroller determines scaled error according to

$$ScaledError = K_i * error[n] + K_a * \sum_{i=1}^{n} error[i],$$

where K_i is a coefficient for scaling the instantaneous error and K_a is a coefficient.

Claims 14 and 15 (canceled)

Claim 16 (original): A method for producing a timing distribution signal comprising the steps of:

removing jitter from a signal with a first filter; and

removing wander from the signal with a second filter separate and apart from the first filter.

Claim 17 (original): A method as described in Claim 16 wherein the removing the jitter step includes the step of applying an error correction signal to a direct digital synthesizer of the first filter by a first microcontroller of the first filter based on accumulated error between a reference input clock signal and a clock signal from the direct digital synthesizer.

Claim 18 (original): A method as described in Claim 17 wherein before the removing the jitter step, there is the step of producing the clock signal from the signal from an oscillator.

Claim 19 (original): A method as described in Claim 18 wherein the applying step includes the step of applying dither to the accumulated error.

Claim 20 (original): A method as described in Claim 19 wherein the removing wander step includes the step of applying a second error correction signal to a second direct digital synthesizer of the second filter by a second microcontroller based on accumulated error for a predetermined period of time between the clock signal and a second clock signal from the second direct digital synthesizer.

Claim 21 (original): A method as described in Claim 20 wherein before the applying dither step of the applying step, there is the step of computing an average error value.

Claim 22 (original): A method as described in Claim 21 wherein after the computing step of the applying step, there is the step of computing a scaled error value where

$$ScaledError = K_i * error[n] + K_a * \sum_{i=1}^{n} error[i],$$

where K_i is a coefficient for scaling the instantaneous error and K_a is a coefficient.

Claim 23 (original): A method as described in Claim 22 wherein before the average error value computing step, there is the step of comparing counts of a first counter counting a second predetermined number of cycles between rising edges of the reference input

clock signal and of a second counter counting the second predetermined number of cycles between rising edges of the clock signal.

Claim 24 (canceled)

Claim 25 (original): A method for producing a timing distribution signal comprising the steps of:

producing the timing distribution signal, a first master signal and a second master signal with a master hardware system;

receiving the first master signal, second master signal and timing distribution signal at a back up hardware system which informs the backup hardware system that the master hardware system is a master over the backup hardware system, it is in either a failed or non-failed condition, and which the back up hardware system uses as a reference signal but the backup hardware system does not transmit any timing distribution signal if it is not the master, respectively;

entering the master hardware system in a failed condition; and

having the backup hardware system immediately becoming the master and continuing to transmit the timing distribution signal that the master hardware system was transmitting before the master hardware system failed and stopped transmitting its timing distribution signal, with the timing distribution signal from the backup hardware system aligned with the timing distribution signal provided by the master hardware system before it failed so there is no phase discontinuity when the backup hardware system becomes the master and begins transmitting the timing distribution signal.

Claim 26 (original): A timing distribution apparatus comprising:

a master hardware system and a backup hardware system for the master hardware system that allows the master hardware system to fail without any phase discontinuity, each hardware system comprising: a first filter for removing jitter from the signal; and a second filter for removing wander from the signal separate and apart from the first filter; the master hardware system having a first master signal and a second master signal that are sent to the back up hardware system that informs the backup hardware system that the master hardware system is a master over the backup hardware system and, it is either in a failed or non-failed condition, respectively, the master hardware system producing a timing distribution signal that is sent to the backup hardware system which the backup hardware system uses as a reference signal for the backup hardware system but the backup hardware

system does not transmit any timing distribution signal if it is not the master, wherein when the master hardware system enters a failed condition, the backup hardware system immediately becomes the master and the backup hardware system continues to transmit the timing distribution signal that the master hardware system was producing before it failed with the timing distribution signal from the backup hardware system aligned with the timing distribution signal produced by the master hardware system before it failed so there is no phase discontinuity.

Claim 27 (previously presented): A timing distribution apparatus comprising:

a source for producing a signal;

a first filter for removing jitter from the signal, the first filter includes a first tuneable directed digital synthesizer connected to the source for producing a clock signal derived from the signal from the source, the first filter includes a reference input clock signal mechanism for providing a reference input clock signal with respect to the clock signal, the first filter includes a microcontroller which accumulates error between the clock signal and a reference input clock signal and produces an error correction signal to tune the directed digital synthesizer, the accumulated error includes a scaled error, and the first microcontroller determines scaled error according to

$$ScaledError = K_i * error[n] + K_a * \sum_{i=1}^{n} error[i],$$

where K_i is a coefficient for scaling the instantaneous error and K_a is a coefficient; and

a second filter for removing wander from the signal separate and apart from the first filter.